Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.066”**

**SOURCE**

**.085”**

**GATE**

**.020 x .025”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: DRAIN**

**Mask Ref: GEN 5**

**APPROVED BY: DK DIE SIZE .066” X .085” DATE: 9/28/22**

**MFG: INT’L RECTIFIER THICKNESS .012” P/N: IRLC024NB**

**DG 10.1.2**

#### Rev B, 7/1